WHAT IS CLAIMED IS:

1. A circuit to access unstored data comprising:

a register file;

a first bi-directional OR controller connected to said register file;

a first multiplexer having a first input connected to an output of said first bi-directional OR controller;

a second bi-directional OR controller connected to said register file;

a second multiplexer having a first input connected to an output of said second bi-directional OR controller; and

a control circuit connected to said first bi-directional OR controller and said second bi-directional OR controller.

2. A circuit according to claim 1 further comprising:

a first latch having an output connected to a first input of said first bi-directional OR controller; and

a second latch having an output connected to a first input to said second bi-directional OR controller.

3. A circuit according to claim 2 further comprising:

a first functional unit having a first output connected to a second input to said first multiplexer and having a second output connected to an input to said first latch.

4. A circuit according to claim 3 further comprising:

a second functional unit having a first output connected to a second input of said second multiplexer and having a second output connected to an input of said second latch.

5. A circuit according to claim 4 wherein:

said first multiplexer is part of a first data forwarding circuit; and

said second multiplexer is part of a second data forwarding circuit.

6. A circuit according to claim 5 wherein said control circuit determines whether the output from said first bi-directional OR controller is sent across said register file to said second bi-directional OR controller or if the output from said second bi-directional OR controller is sent across said file register to said first bi-directional OR controller.

7. A circuit according to claim 6 wherein said first bi-directional OR controller is a first bi-directional wired OR controller; and

said second bi-directional OR controller is a second bi-directional wired OR controller.

8. A circuit according to claim 6 wherein said first bi-directional OR controller is a first bi-directional wired OR controller; and

said second bi-directional OR controller is a second bi-directional wired OR controller.

9. A circuit according to claim 6 further comprising:

one or more latches between a source of unstored data and said first bi-directional OR controller.

10. A circuit according to claim 8 further comprising:

one or more latches between a source of unstored data and said second bi-directional OR controller.

11. The circuit according to claim 6 further comprising:

one or more latches between a source of unstored data and said first bi-directional controller; and

one or more latches between a source of unstored data and said second bi-directional controller.

12. A circuit according to claim 6 further comprising:

one or more additional bi-directional OR controllers having a bi-directional connection across said register file.

13. A circuit according to claim 6 further comprising:

one or more additional bi-directional OR controllers having a bi-directional connection to said first bi-directional OR controller or to said second bi-directional OR controller wherein the connection does not go across said register file.

14. An encoded multiplexer comprising:

a first input with at least one instance;

a second input with at least one instance;

a first raw select signal with at least one instance;

a second raw select signal with at least one instance; and

a circuit which combines said first raw select signal and said second raw select signal to determine which input should be used as a first conditioned select signal and a second conditioned select signal.

15. An encoded multiplexer according to claim 14 wherein said circuit comprises:

an OR gate having said first raw select signal as an input;

an invertor having an input connected to an output of said OR gate; and

a nand gate having a first nand input connected to an output of said invertor and a second nand input connected to said second raw select signal input.

16. An encoded multiplexer according to claim 15 wherein said first conditioned select signal is connected to said first raw select signal; and

said second conditioned select signal is connected to the output of the nand gate.

17. An encoded multiplexer according to claim 16 wherein said first raw select signal is connected to the select signal from a previous cycle; and

said second raw select signal is connected to the select signal from the cycle before the previous cycle.

18. An encoded multiplexer comprising:

a first input with at least one instance;

a second input with at least one instance;

a first raw select signal with at least one instance;

a second raw select signal with at least one instance; and

a circuit which combines said first raw select signal and said second raw select signal to determine which input should be used as a first conditioned select signal, a second conditioned select signal and a third conditioned select signal.

19. An encoded multiplexer according to claim 18 wherein said circuit comprising:

a first NAND gate having an input A connected to said second raw select input;

a first OR gate having an input B connected to said first raw select input and an input C connected to an output of said first NAND gate;

a second OR gate having an input D connected to said first raw select input;

a invertor having an input connected to the output of said second OR gate; and

said first NAND gate having an input E connected to an output of said invertor.

20. An encoded multiplexer according to claim 19 wherein said first conditioned select signal is connected to a current select signal;

said second conditioned select signal is connected to an output of said second OR gate; and

said third conditioned select signal is connected to an output of said invertor.